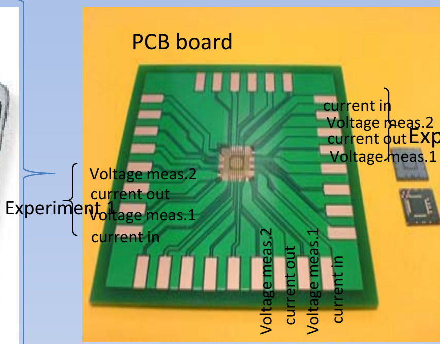
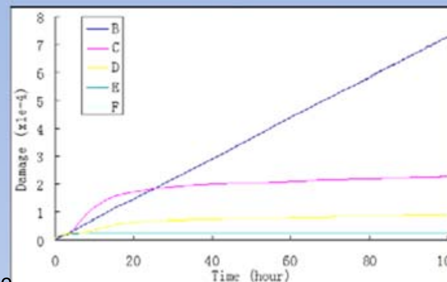
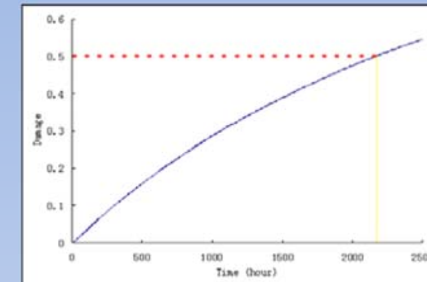
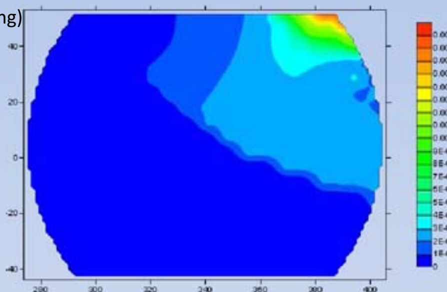
A Multi-Scale Damage Mechanics Framework for Nanoelectronics Interconnects and Solder Joints

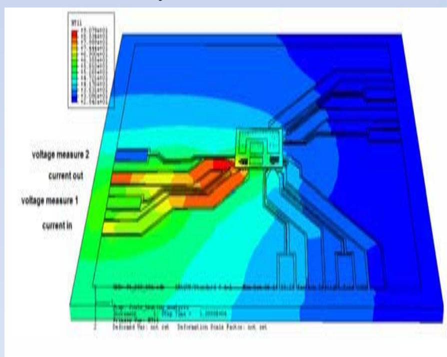


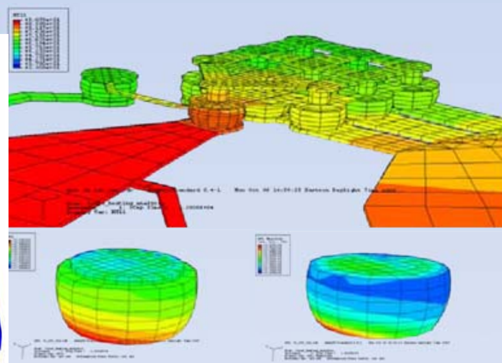






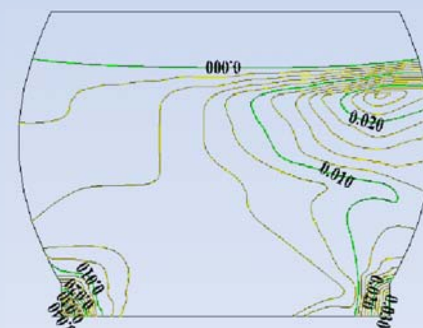
With insatiate demand for miniaturization, electromigration and thermomigration turn to be the major reliability concern. Coupled thermal electrical analysis of flip chip solder bump was conducted in Electric Package Laboratory.





Electronic Package Board Modeling under Current Load

Temperature Contour



Damage Contour

- How temperature region (C, D, E, F) damage cease to increase after some period
- When the temperature gradient exceeds a threshold, damage will keep accumulating until it fails.
- Software required: ABAQUS, MATLAB, FORTRAN, LAMMPS
- Equipment Required: Nano Indenter, Thermal Couple, Thermal Meter, Function Generator, DC Power Supply, Thermal Chamber
- Future Research: With more and more IC connectors begin to carry pulsed DC under normal operating conditions, degradation physics of solder under such load condition is still quite limited. Electromigration and thermomigration analysis of solder under pulsed DC will be conducted in the Lab.

UB EPL *Buffalo*

NRL *Tabuk*